Index

IEE Proceedings
Computers and Digital Techniques
Vol. 148, 2001

Author Index

A

Aborhey, S. p63
Al-Hashimi, B.M. p163
Aoki, T. p196
Aso, H. p141

B

Baidas, Z. p31
Bandyopadhyay, S. p238
Brown, A.D. p31
Burgess, N. p49
Buzluca, F. p15

C

Casinovi, G. p129
Chang, J.M. p167
Chang, T.-S. p227
Chattopadhyay, S. p147
Chen, D. p196
Chiu, J.-C. p113
Chung, C.-P. p113

D

Deng, X. p101
Diessel, O. p152
Dlay, S.S. p221

F

Falkowski, B.J. p7, p71

G

Green, D.H. p53
Green, P.R. p53

H

Hamalainen, T. p23
Harmanci, E. p15
Harrison, P.G. p176
He, W.-H. p139
Higuchi, T. p196
Hinton, O.R. p221
Homma, N. p196

I

Imana, J.L. p189
Imitaz, A. p79

J

Jen, C.-W. p227
Jou, J.-Y. p1

K

Kannurao, S. p71
Knottenbelt, W.J. p176
Kuusilinna, K. p23

L

Lahtinen, V. p23
Lee, C.H. p101
Lee, J.-Y. p95
Lee, S. p141
Lin, G.J. p119
Liu, C.-N. p1
Lo, C.-T.D. p167
Loucif, S. p89
Luk, W. p105

M

Martin, K.M. p45
Maulik, U. p238
Milne, G. p152
Min, G. p215

N

Nakahara, J., Jr. p45
Nicolici, N. p163

O

Omachi, S. p141
Ould-Khaoua, M. p89, p215

R

Rahardja, S. p7
Roy, S. p238

S

Saarinen, J. p23
Sanchez, J.M. p189
Sarbazi-Azad, H. p89
Shao, Z. p233
Sheu, T.L. p119
Srisa-an, W. p167

W

Wajdi, T. p79
Wallace, W.F. p221
Weinhaudt, M. p105
Williams, A.C. p31
Woods, S. p129
Wu, T.-S. p139

Y

Yen, S.-M. p207

Z

Zertal, S. p176
Zhu, H. p101

AUTOMATA THEORY

Efficient coverage analysis metric for HDL design validation p1
Finite state machine encoding for VHDL synthesis p23
Low power state assignment and flipflop selection for finite state machine synthesis - a genetic algorithmic approach p147

CIRCUIT THEORY AND DESIGN

Formulation for the computation of Boolean operations p189
Hardware compiler realising concurrent processes in reconfigurable logic p152
Low power state assignment and flipflop selection for finite state machine synthesis - a genetic algorithmic approach p147
Pragmatic method for the design of fast constant coefficient combinational multipliers p196
Probabilistic carry state estimate for improved asynchronous adder performance p221
Proof regarding the NP-completeness of the unweighted complex-triangle elimination (CTE) problem for general adjacency graphs p238

CODES AND DECODING

Polyphase related-prime sequences p53
Reed-Muller tree-based minimisation of fixed polarity Reed-Muller expansions p63

COMMUNICATION SYSTEM THEORY

Deniable authentication protocols p101
Weaknesses of protocols for updating the parameters of an established threshold scheme p45

COMPUTATIONAL COMPLEXITY

Analysis of disjoint decomposition of balanced Boolean functions through the Walsh spectrum p71
Low power state assignment and flipflop selection for finite state machine synthesis - a genetic algorithmic approach p147
Optimal algorithm for tree scheduling with unit time communication delays p79
Performance analysis of three implementation strategies for distributed lock management p176
PLI logic for multiple-valued functions p7
Proof regarding the NP-completeness of the unweighted complex-triangle elimination (CTE) problem for general adjacency graphs p238
Reed-Muller tree-based minimisation of fixed polarity Reed-Muller expansions p63

COMPUTER COMMUNICATIONS

Dynamic synchronous bandwidth allocation scheme for hard real-time communication in FDDI networks p15
Multiple-path ATM switch architecture for dynamic VC establishment p119
Optimal algorithm for tree scheduling with unit time communication delays p79
PayFair: a prepaid internet ensuring customer fairness micropayment scheme p207
Pragmatic method for the design of fast constant coefficient combinational multipliers p196

COMPUTER GRAPHICS

VLSI architecture for quadtree-based fractal image coding p141

COMPUTERISED INSTRUMENTATION

Minimising power dissipation in partial scan sequential circuits p163

DATA COMMUNICATION

Deniable authentication protocols p101
Dynamic synchronous bandwidth allocation scheme for hard real-time communication in FDDI networks p15
Weaknesses of protocols for updating the parameters of an established threshold scheme p45

DATA HANDLING

Performance analyses on the generalised buddy system p167
VLSI architecture for quadtree-based fractal image coding p141

DATA SECURITY

Comment on Lin-Wu (t, n)-threshold verifiable multisecret sharing scheme p139
Cryptographic systems using a self-certified public key based on discrete logarithms p233
Deniable authentication protocols p101
PayFair: a prepaid internet ensuring customer fairness micropayment scheme p207
Threshold signature scheme with multiple signing policies p95
Weaknesses of protocols for updating the parameters of an established threshold scheme p45

DIGITAL ARITHMETIC

Efficient RNS-to-binary conversion using high-radix SRT division p49
Pragmatic method for the design of fast constant coefficient combinational multipliers p196
Probabilistic carry state estimate for improved asynchronous adder performance p221

DIGITAL FILTERS

Hardware-efficient pipelined programmable FIR filter design p227

DIGITAL TECHNIQUES

Memory access optimisation for reconfigurable systems p105

ENGINEERING COMPUTING

Formulation for the computation of Boolean operations p189
Hardware compiler realising concurrent processes in reconfigurable logic p152
High-bandwidth x86 instruction fetching based on instruction pointer table p113
Low power state assignment and flipflop selection for finite state machine synthesis - a genetic algorithmic approach p147
Memory access optimisation for reconfigurable systems p105
Multiple-level logic simulation algorithm p129
Pragmatic method for the design of fast constant coefficient combinational multipliers p196
Probabilistic carry state estimate for improved asynchronous adder performance p221
Proof regarding the NP-completeness of the unweighted complex-triangle elimination (CTE) problem for general adjacency graphs p238

FEEDBACK

Multiple-level logic simulation algorithm p129

FORMAL LOGIC

Analysis of disjoint decomposition of balanced Boolean functions through the Walsh spectrum p71
Formulation for the computation of Boolean operations p189
Hardware compiler realising concurrent processes in reconfigurable logic p152
Multiple-level logic simulation algorithm p129
PLI logic for multiple-valued functions p7
Polyphase related-prime sequences p53
Reed-Muller tree-based minimisation of fixed polarity Reed-Muller expansions p63
Threshold signature scheme with multiple signing policies p95

INFORMATION THEORY

Reed-Muller tree-based minimisation of fixed polarity Reed-Muller expansions p63

INTEGRATED CIRCUITS

Proof regarding the NP-completeness of the unweighted complex-triangle elimination (CTE) problem for general adjacency graphs p238
VLSI architecture for quadtree-based fractal image coding p141

LOGIC CIRCUITS

Analysis of disjoint decomposition of balanced Boolean functions through the Walsh spectrum p71
Hardware compiler realising concurrent processes in reconfigurable logic p152
Low power state assignment and flipflop selection for finite state machine synthesis - a genetic algorithmic approach p147
Memory access optimisation for reconfigurable systems p105
Minimising power dissipation in partial scan sequential circuits p163
Multiple-level logic simulation algorithm p129
Pragmatic method for the design of fast constant coefficient combinational multipliers p196
Probabilistic carry state estimate for improved asynchronous adder performance p221

LOGIC DESIGN

Efficient coverage analysis metric for HDL design validation p1
Finite state machine encoding for VHDL synthesis p23
Formulation for the computation of Boolean operations p189
Hardware compiler realising concurrent processes in reconfigurable logic p152
High-bandwidth x86 instruction fetching based on instruction pointer table p113
Low power state assignment and flipflop selection for finite state machine synthesis - a genetic algorithmic approach p147
Memory access optimisation for reconfigurable systems p105
Minimising power dissipation in partial scan sequential circuits p163
Multiple-level logic simulation algorithm p129
Optimisation in behavioural synthesis using hierarchical expansion: module ripping p31
Pragmatic method for the design of fast constant coefficient combinational multipliers p196
Probabilistic carry state estimate for improved asynchronous adder performance p221

MATHEMATICAL TECHNIQUES

Formulation for the computation of Boolean operations p189
Optimal algorithm for tree scheduling with unit time communication delays p79
Proof regarding the NP-completeness of the unweighted complex-triangle elimination (CTE) problem for general adjacency graphs p238
VLSI architecture for quadtree-based fractal image coding p141

MICROPROCESSORS

High-bandwidth x86 instruction fetching based on instruction pointer table p113

MULTIPROCESSOR SYSTEMS

Circuit switching: an analysis for k-ary n-cubes with virtual channels p215
Message latency in k-ary n-cubes with hop-based routing p89

Performance analysis of three implementation strategies for distributed lock management p176

OPTICAL COMMUNICATION

Dynamic synchronous bandwidth allocation scheme for hard real-time communication in FDDI networks p15

OPTICAL IMAGE PROCESSING

Hardware-efficient pipelined programmable FIR filter design p227
VLSI architecture for quadtree-based fractal image coding p141

OPTIMISATION

Low power state assignment and flipflop selection for finite state machine synthesis - a genetic algorithmic approach p147
Optimisation in behavioural synthesis using hierarchical expansion: module ripping p31
Reed-Muller tree-based minimisation of fixed polarity Reed-Muller expansions p63

PARALLEL PROCESSING

Hardware compiler realising concurrent processes in reconfigurable logic p152
Hardware-efficient pipelined programmable FIR filter design p227
Message latency in k-ary n-cubes with hop-based routing p89
Optimal algorithm for tree scheduling with unit time communication delays p79
PayFair: a prepaid internet ensuring customer fairness micropayment scheme p207
Performance analysis of three implementation strategies for distributed lock management p176
Pragmatic method for the design of fast constant coefficient combinational multipliers p196

PATTERN RECOGNITION

VLSI architecture for quadtree-based fractal image coding p141

PERFORMANCE EVALUATION

Circuit switching: an analysis for k-ary n-cubes with virtual channels p215
Performance analysis of three implementation strategies for distributed lock management p176

PROGRAMMING THEORY

Message latency in k-ary n-cubes with hop-based routing p89

SIGNAL PROCESSING

Analysis of disjoint decomposition of balanced Boolean functions through the Walsh spectrum p71
VLSI architecture for quadtree-based fractal image coding p141

SOFTWARE TECHNIQUES

Performance analyses on the generalised buddy system p167
Performance analysis of three implementation strategies for distributed lock management p176

SWITCHING SYSTEMS

Multiple-path ATM switch architecture for dynamic VC establishment p119

SWITCHING THEORY

Efficient coverage analysis metric for HDL design validation p1
Finite state machine encoding for VHDL synthesis p23
Low power state assignment and flipflop selection for finite state machine synthesis - a genetic algorithmic approach p147
Multiple-path ATM switch architecture for dynamic VC establishment p119
Performance analysis of three implementation strategies for distributed lock management p176
PLI logic for multiple-valued functions p7